**Lab Report : 02**

# Title: Design and logic verification of combinational circuit of y=AB+CD using µ-wind

# 

# Course title:VLSI Circuits Design Lab.

Course code: CSE-412

4th Year1st Semester

**Date of Submission : 1-12-1015**

**Submitted to-**

**Abu Sayed Md. Mostafizur Rahaman**

**Associate Professor**

**Department of Computer Science and Engineering**

**Jahangirnagar University**

**Amina Khatun**

**Lecturer**

**Department of Computer Science and Engineering**

**Jahangirnagar University**

**Submitted by-**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | *Class Roll* | *Exam Roll* | *Name* | *Session* | *Signature* |
|  | 407 | 120103 | Aditi Sarker | 2011-12 |  |